ABSTRACT OF THE DISCLOSURE

A system and method of calibrating a digital-to-analog converter (DAC) such as a resistor string DAC that reduces costs by making more efficient use of semiconductor die area. A digital-to-analog converter includes a main DAC to be calibrated, a memory, a plurality of calibration DACs, and an analog summing circuit. The main DAC receives digital input code values, and converts the respective input code values into an analog signal. A first calibration DAC receives a predetermined number of lower order bits of the respective input code values, and interpolates between a positive reference voltage and a negative reference voltage to generate linear waveforms for the PWL approximation. A second calibration DAC generates the positive reference voltage, and a third calibration DAC generates the negative reference voltage. The memory stores a plurality of PWL breakpoint code values representing respective integral non-linearity error values of the main DAC, and applies consecutive PWL breakpoint code values to the second and third calibration DACs, respectively, to generate the positive and negative reference voltages for the first calibration DAC.

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ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313